

# FDFMA3P029Z

## Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

-30 V, -3.3 A, 87 mΩ

### Features

#### MOSFET

- Max  $r_{DS(on)}$  = 87 mΩ at  $V_{GS} = -10$  V,  $I_D = -3.3$  A
- Max  $r_{DS(on)}$  = 152 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -2.3$  A
- HBM ESD protection level > 2 KV typical (Note 3)

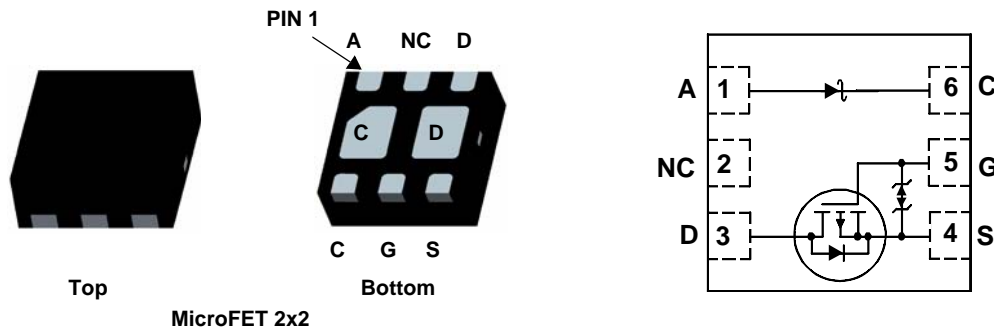
#### Schottky

- $V_F < 0.37$  V @ 500 mA
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant

### General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features a MOSFET with very low on-state resistance and an independently connected low forward voltage schottky diode allows for minimum conduction losses.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	$\pm 25$	V
$I_D$	Drain Current -Continuous (Note 1a)	-3.3	A
	-Pulsed	-15	
$P_D$	Power Dissipation (Note 1a)	1.4	W
	(Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
$V_{RRM}$	Schottky Repetitive Peak Reverse Voltage	20	V
$I_O$	Schottky Average Forward Current	2	A

### Thermal Characteristics

Symbol	Parameter	Rated	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	86	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	86	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	173	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3P2	FDFMA3P029Z	MicroFET 2X2	7"	8 mm	3000 units

### Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = -10\text{ V}$ , $I_D = -3.3\text{ A}$		69	87	m $\Omega$
		$V_{GS} = -4.5\text{ V}$ , $I_D = -2.3\text{ A}$		108	152	
		$V_{GS} = -10\text{ V}$ , $I_D = -3.3\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		97	122	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}$ , $I_D = -3.3\text{ A}$		6		S
$R_g$	Gate Resistance			12		$\Omega$

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		324	435	pF
$C_{oss}$	Output Capacitance			59	80	pF
$C_{rss}$	Reverse Transfer Capacitance			53	80	pF

#### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}$ , $I_D = -3.3\text{ A}$ $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		5.2	11	ns
$t_r$	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			17	31	ns
$t_f$	Fall Time			11	25	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$	$V_{DD} = -15\text{ V}$ , $I_D = -3.3\text{ A}$	7.2	10
	Total Gate Charge	$V_{GS} = 0\text{ V to } -5\text{ V}$	4.1		6	nC
$Q_{gs}$	Gate to Source Gate Charge			1.0		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.9		nC

#### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -3.3\text{ A}$ (Note 2)		-0.94	-1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = -3.3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		20	32	ns
$Q_{rr}$	Reverse Recovery Charge			10	18	nC

#### Schottky Diode Characteristics

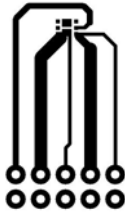
$V_R$	Reverse Voltage	$I_R = 1\text{ mA}$	$T_J = 25\text{ }^\circ\text{C}$	20			V
$I_R$	Reverse Leakage	$V_R = 20\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		30	300	$\mu\text{A}$
			$T_J = 125\text{ }^\circ\text{C}$		10	45	mA
$V_F$	Forward Voltage	$I_F = 500\text{ mA}$	$T_J = 25\text{ }^\circ\text{C}$		0.32	0.37	V
			$T_J = 125\text{ }^\circ\text{C}$		0.21	0.26	
		$I_F = 1\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$		0.37	0.435	
			$T_J = 125\text{ }^\circ\text{C}$		0.28	0.33	

**Notes:**

- 1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
- (a) MOSFET  $R_{\theta JA} = 86$  °C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
  - (b) MOSFET  $R_{\theta JA} = 173$  °C/W when mounted on a minimum pad of 2 oz copper
  - (c) Schottky  $R_{\theta JA} = 86$  °C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB.
  - (d) Schottky  $R_{\theta JA} = 173$  °C/W when mounted on a minimum pad of 2 oz copper.



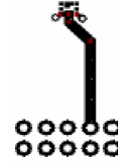
a) 86 °C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper.



b) 173 °C/W when mounted on a minimum pad of 2 oz copper.



c) 86 °C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper.

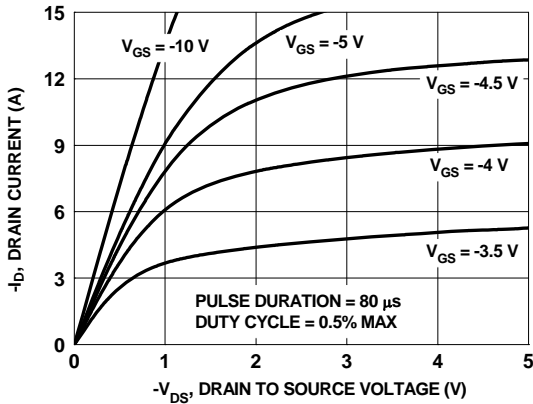


d) 173 °C/W when mounted on a minimum pad of 2 oz copper.

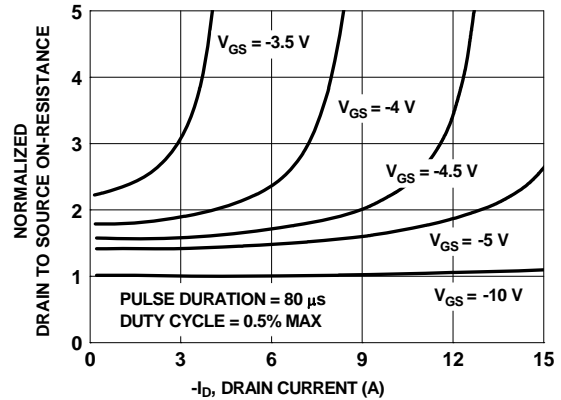
2: Pulse Test : Pulse Width < 300 μs, Duty Cycle < 2.0%

3: The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

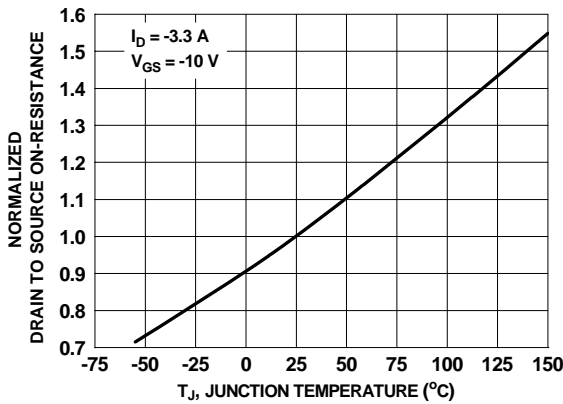
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



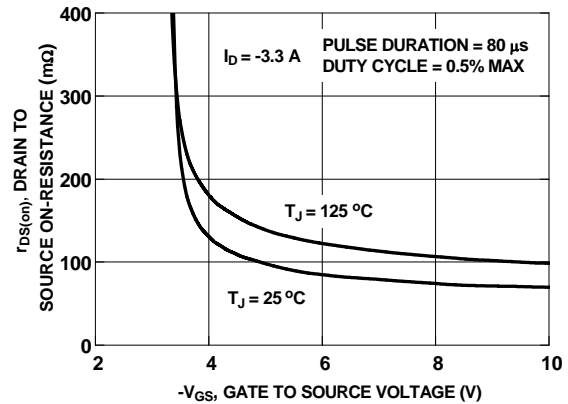
**Figure 1. On-Region Characteristics**



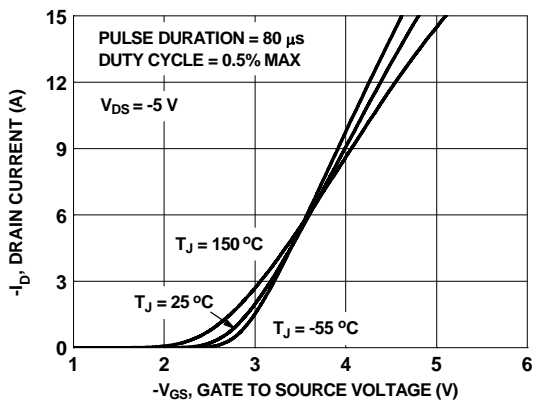
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



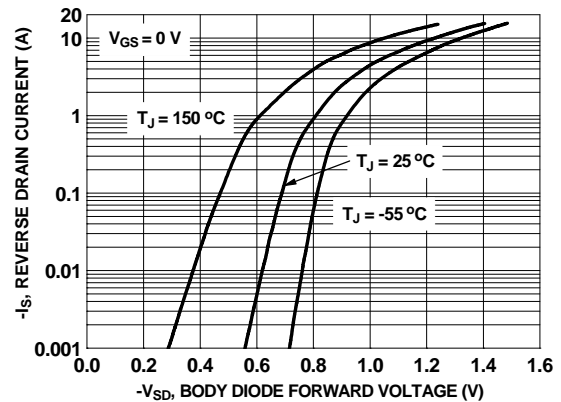
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

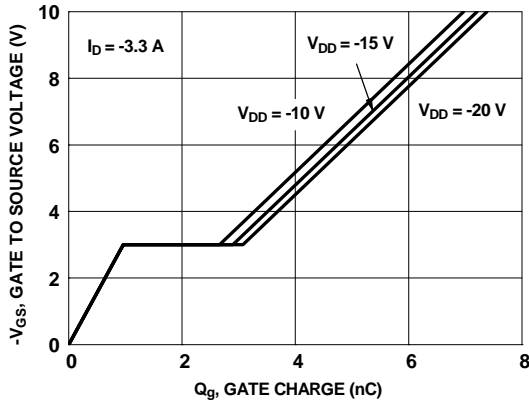


**Figure 5. Transfer Characteristics**

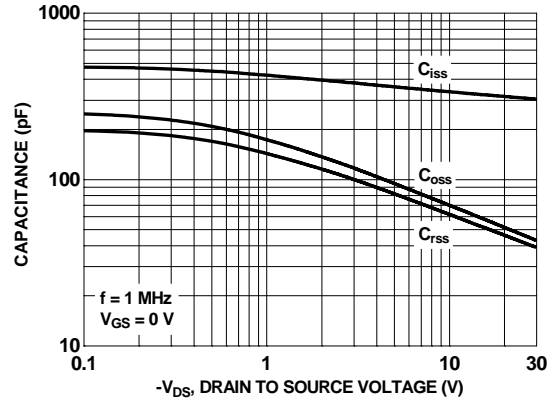


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

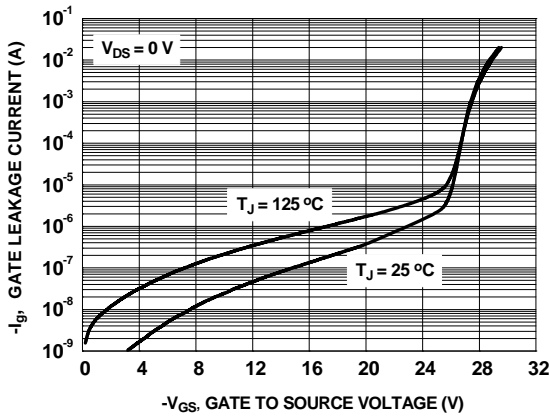
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



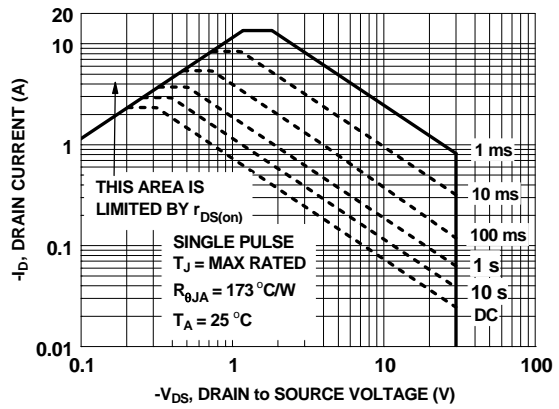
**Figure 7. Gate Charge Characteristics**



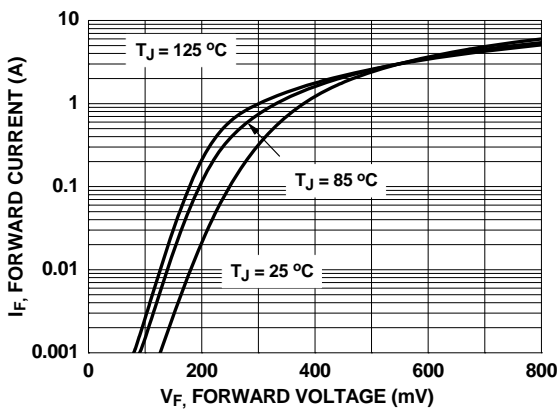
**Figure 8. Capacitance vs Drain to Source Voltage**



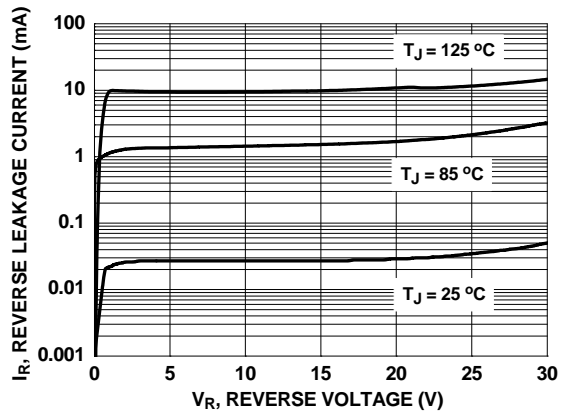
**Figure 9. Gate Leakage Current vs Gate to Source Voltage**



**Figure 10. Forward Bias Safe Operating Area**

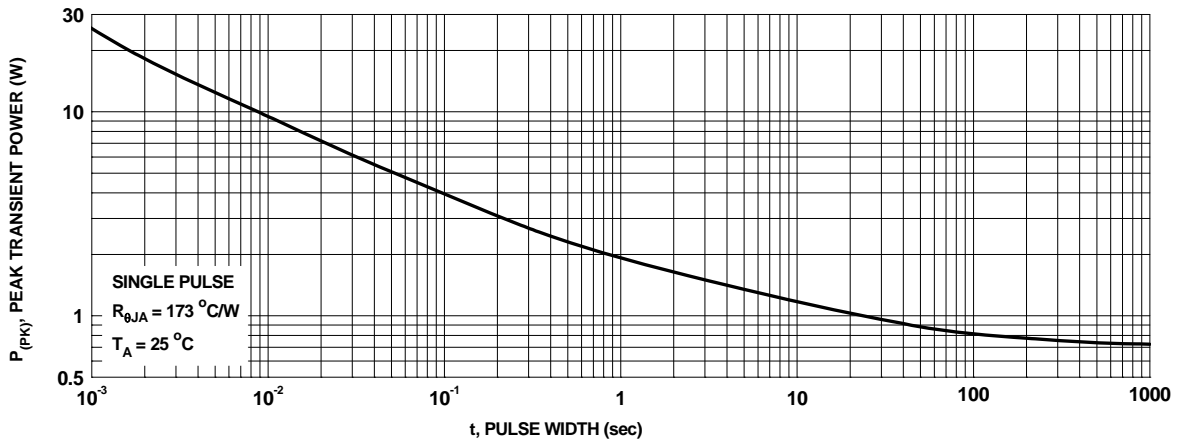


**Figure 11. Schottky Diode Forward Voltage**

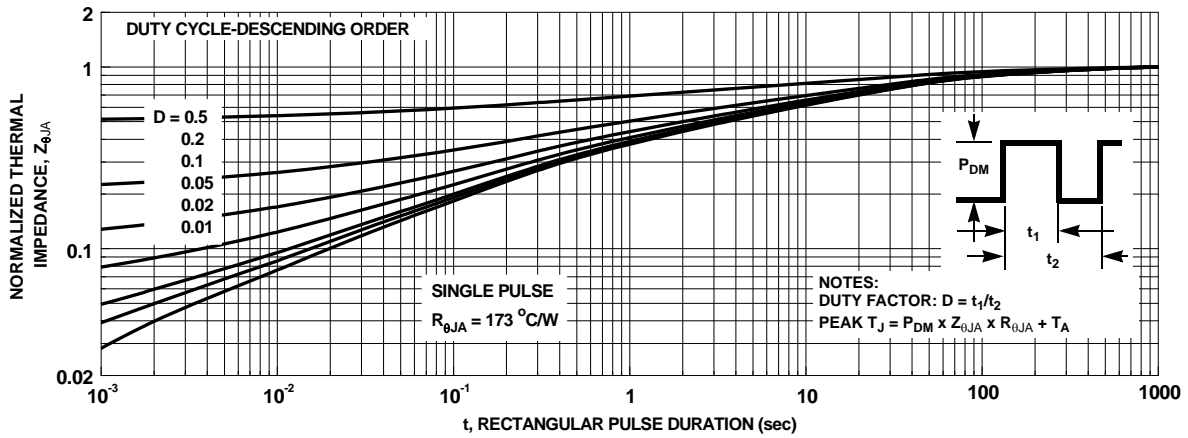


**Figure 12. Schottky Diode Reverse Current**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

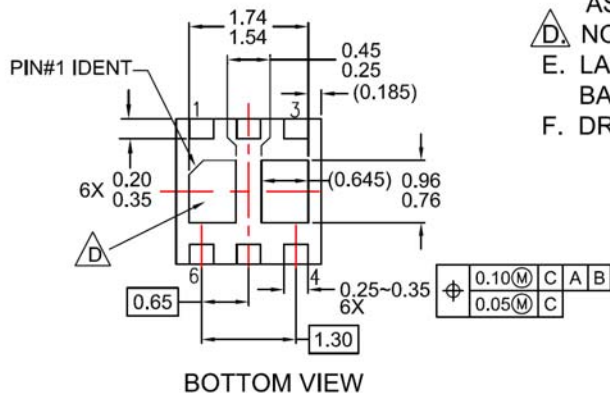
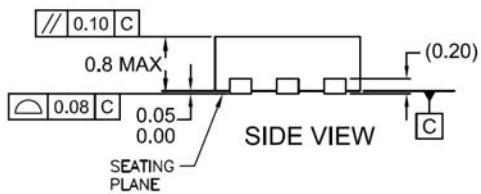
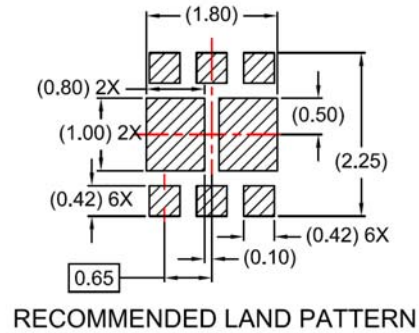
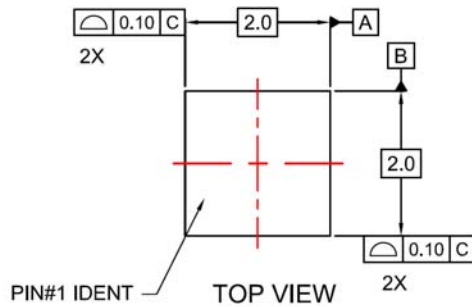


**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout








### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. NON-JEDEC DUAL DAP
- E. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- F. DRAWING FILENAME: MKT-MLP06Jrev3.



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